CLAIMS

What is claimed is:

1. A method comprising:
translating a virtual memory address into a physical memory address, the translating including,
creating a first page size tag;
choosing an entry in a translation lookaside buffer, wherein the entry stores a second page size tag and a page frame number;
comparing the first page size tag with the second page size tag; and
if the first page size tag is equal to the second page size tag, using the page frame number to form the physical memory address.

2. The method of claim 1, wherein the translating further includes,
if the first page size tag is greater then the second page size tag, generating a miss indication.

3. The method of claim 1, wherein the translation lookaside buffer is N-way set associative.

4. The method of claim 1, wherein the translation lookaside buffer is a second level translation lookaside buffer.

5. The method of claim 1, wherein the page size tag is represented in a 4-bit string.

6. A method comprising:
searching a translation lookaside buffer (TLB) to resolve a virtual memory address, wherein the TLB includes a plurality of entries, and wherein one or more of the entries include a TLB page size tag and a page frame number, the searching including,
comparing a first page size tag with the TLB page size tag of an entry in the TLB, wherein the first page size tag is selected from a search order list; and

after determining the first page size tag is less than or equal to the TLB page size tag, writing the page frame number to a predetermined memory location;

after determining the page size tag is greater than to the TLB page size comparing a second page size tag with the TLB page size tag of the entry, wherein the second page size tag is selected from the search order list.

7. The method of claim 6, wherein the translating further includes,

after determining the page size tag is greater than the TLB page size tag, generating a miss indication.

8. The method of claim 6, wherein the translation lookaside buffer is N-way set associative.

9. The method of claim 6, wherein the translation lookaside buffer is a second level translation lookaside buffer.

10. The method of claim 6, wherein the page size tag is represented in a 4-bit string.

11. An apparatus comprising:

a translation lookaside buffer (TLB), the TLB including a plurality of entries, the entries including,

a TLB page size tag field; and

a page frame number field;

a search list unit to transmit a page size tag based on a search list;

a selection logic to select an entry of the plurality of entries based on the page size tag; and

a comparator to compare the page size tag with the contents of the TLB page size tag field of the selected entry.

12. The apparatus of claim 11, wherein the TLB is a second-level N-way set associative TLB.

13. The apparatus of claim 11, wherein the search list unit is updated according to a least recently used policy.

14. The apparatus of claim 11, wherein the comparator generates a hit indication if the page size tag matches the contents of the TLB page size tag field.

15. The apparatus of claim 11, wherein the comparator generates a miss indication if the page size tag is greater than the contents of the TLB page size tag field.

16. A system comprising:
a random access memory (RAM) unit;
a processor coupled with the RAM unit, the processor including,
a translation lookaside buffer, the translation lookaside buffer (TLB) including,
a plurality of entries, the plurality of entries including,
a TLB page size tag field; and
a page frame number field.

17. The system of claim 16 further comprising:
a page size encoder to produce a page size tag;
a selection logic to select one of the plurality of entries of the TLB, wherein the selection is based on the page size tag; and
a comparitor to compare the page size tag with the contents of the TLB page size tag field of the selected entry.

18. The system of claim 16, wherein the TLB is set-associative.

19. The system of claim 16, wherein the TLB is a second-level TLB.

20. The system of claim 16, wherein the plurality of entries further include a TLB global field and a TLB application specific identifier field.